A G3-PLC Network Simulator with Enhanced Link Level Modeling

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Abstract

This work presents a G3-PLC network simulator for Smart Metering applications. Its main features are the use of a distributed event-based approach, the implementation of the layer 2+ stack using the same code embedded in actual Microchip G3-PLC devices and an enhanced modeling of the communication channel and the physical layer. The simulator is validated by comparing its results with the ones obtained in a test network deployed in the laboratory.

Index Terms

Smart Metering, G3-PLC, network simulation, link level, effective signal-to-interference-and-noise ratio.

I. Introduction

A Smart Metering network is the integrated set of management elements and communication network that allows the remote consumption reading, the diagnosis and the on/off switching of electricity meters. The G3-PLC specification defines a suitable system for this purpose [1].

In this context, network simulators are very useful tools for developing and debugging the communication stack, for assessing and improving their performance and for solving problems that arise in actual deployments. This work presents a G3-PLC network simulator based on the framework proposed in [2], but in which the abstraction of the communication channel and of the physical layer has been enhanced to achieve a more accurate modeling while allowing faster than real-time simulation of complex networks.

II. G3-PLC network simulator

A. Simulator architecture

The employed architecture is based on the proposal given in [2]. Each G3-PLC node (including the coordinator) is simulated by an independent process that implements the full stack, except most parts of the physical layer, and an event machine. Layers are implemented employing the same code used in actual G3-PLC devices by Microchip. A Control module that runs in a different process commands the simulation and ensures its coherence by exchanging events with the event machines of the nodes. The latter run concurrently for a time specified by the Control module. Then they stop and send the frame transmission events to the Network process, which implements the physical layer and the shared power line communications (PLC) channel. It processes events from all the nodes and sends the appropriate events to each of them.

B. Link level modeling

The Network module processes transmission requests as shown in Fig. 1. It illustrates the events associated to the transmission of two frames in a simplified scenario with three nodes and the network coordinator. It has been assumed that frames transmitted by node 1 and node 3 reach the coordinator and node 2 with a signal level above the receiver sensitivity. Direct communication between node 1 and node 3 is not possible. Since the channel is idle at the senders location, the Network module sends a TX_START to the senders, indicating that frame is being transmitted, and notifies all the nodes that receive the frame with a signal level above the receiver sensitivity that a frame preamble has been detected (CARRIER_DET). If the frame senders were already receiving a frame (even if it were destined to another node), the Network process would have answered that the channel were busy and transmissions would not have been performed.

In the situation shown in Fig. 1, the Network module determines the destiny of the transmitted frames and estimates the errors due to the channel characteristics and to the possible collisions with other frames. Finally, it notifies the sender that the frame has been transmitted (TX_END); it also informs the destiny that a frame has been received and the occurred errors (FRAME_RX), and communicates that the channel is now idle (CHANNEL_IDLE) to the remaining nodes that were receiving the frame.

Frame errors are computed using the effective signal-to-interference mapping (ESM) function proposed in [3]. The values of β have been computed using the procedure described in [4]. Table I shows the obtained results for the modulations used in the payload. This approach allows simulating frequency selective channels with colored noise. The noise level at each carrier is given by a random variable (RV), which allows modeling the effect of impulsive noise. The mean of this RV can be time-varying. The signal-to-interference-and-noise ratio (SINR) in each carrier is computed taking into account that different modulations are used in the frame control header (FCH) and the payload, as well as the possible collisions with other frames, as shown in Fig. 1.

III. Validation and Network Performance Analysis

The simulator has been validated by comparing its results to the ones obtained in a test network deployed in the laboratory. It consists of the coordinator and 100 nodes distributed in 5 levels. A flat attenuation of 50 dB is introduced between each level and also between the coordinator and the first level. A line impedance stabilization network (LISN) is used to control the noise level in the network, which is fixed to ensure that differential 8PSK modulation can be employed. By doing so, the capacity to simulate the adaptive modulation process defined the G3-PLC specification can be also tested. The application layer emulates the DLMS/COSEM protocol.

Simulation has been executed in a Dell Precision T7600 workstation equipped with two Intel Xeon CPUs (E5-2687W) at 3.10 GHz, 32 Gbytes of RAM and two SAS hard drives. The simulated-time to real-time ratio for the tested network is $17/60$, i.e. faster than real-time. Table II shows the bootstraping time (time for all the nodes to get registered), the average cycle time (time to read the energy consumption of all the nodes) and the maximum number of hops (number of times that a frame is relayed). As seen, there is an excellent matching between the measured and the simulated results.

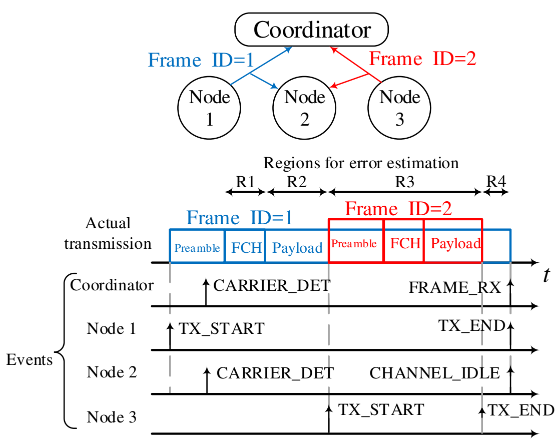

Fig. 1. Simplified transmission example and corresponding events and regions used for errors estimation.

TABLE I
Values of β used in the ESM function in the CENELEC-A/FCC bands

Modulation	Coherent	Differential
Robust BPSK	0.2/0.2	1.4/1.3
BPSK	0.4/0.3	1.1/1.0
QPSK	0.7/0.8	1.6/1.8
8PSK	1.5/1.6	4.2/4.7

TABLE II
Simulated and measured performance values

Performance indicator	Simulated	Measured
Bootstrap time (minutes)	53	52
Average cycle time (s)	680	680
Maximum number of hops	5	5

IV. Conclusion

This work has presented a G3-PLC network simulator. It implements the full stack using the same code that is embedded in actual Microchip G3-PLC devices. Frame errors are estimated using the ESM function, which has been parameterized for the modulations defined in the specification. This allows simulating frequency selective channel responses and colored noise, which can be also time-varying. The computation of the SINR at each carrier takes into account the possible collisions with other frames. The simulator has been validated by comparing their results to a test network deployed in the laboratory consisting of a coordinator and one hundred meters distributed in 5 levels.

References

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